NACT TUTORIAL 0
REFERENCE CLOCK CALIBRATION

Applies to: NACT MODE ONLY

Prerequisites: none

This tutorial takes you through the steps to calibrate the reference clock which is a prerequisite to virtually all NACT operations.

Definitions:

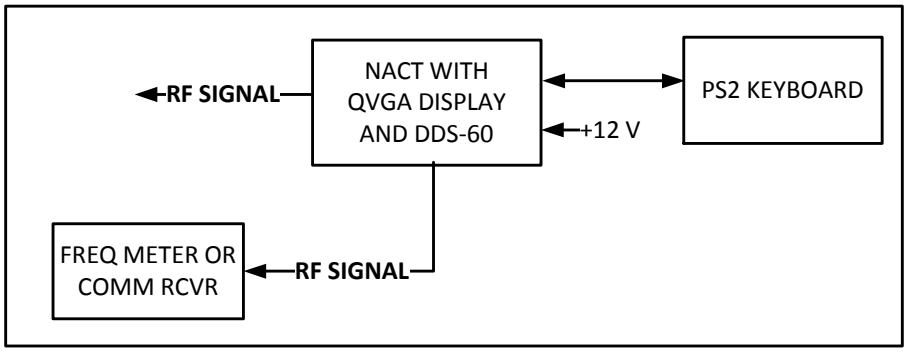
- NAT – **N**etwork **A**nalyzer **T**erminal: Requires PHSNA Arduino (UNO/NANO microcontroller) based controller (or equivalent) with communication over the serial interface. The DDS is under control of the PHANA firmware and the PHSNA firmware reads power levels from the RF Power Meter. The NAT firmware emulates an ASCII terminal and an Excel spreadsheet running the PLX-DAQ macro.
- NACT – **N**etwork **A**nalyzer **C**ontrolling **T**erminal: Does not require a separate controller, uses an on-board DDS-60 to interface direct to the DUT and reads power levels direct from the RF Power Meter. Use of the serial interface is not required. The NACT firmware does everything the NAT firmware does plus all the pertinent functions of the PHSNA controller firmware.

In general, the term NAT will apply to the generic terminal/controller running the Version 3 firmware. NACT functions are activated by the NA Controller mode op mode which is new to Version 3

The minimum requirements for this tutorial are:

- NACT running firmware Version 3.0 or later.
- PS2 Keyboard
- Frequency meter or communications receiver

For this tutorial, the RF output from the DDS is connected to a frequency meter or, if a communications receiver is used to read the RF output frequency, to nothing or, if necessary, a short length of wire to serve as a transmitting antenna. The tutorial is written assuming a communications receiver is used.



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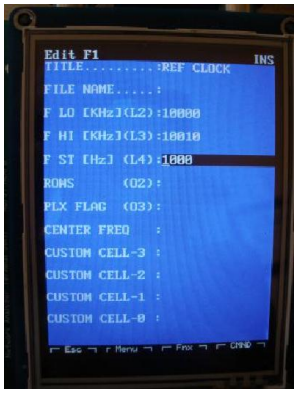
1. Power on all components.
2. Create a PLX data form as follows:
    a. Press Scroll Lock to enter Command mode.
    b. Press F1 to display the data entry form
    c. Set up the F1 PLX form to cover a frequency range of 1 0.000 MHz to 10.005 MHz with 1000 Hz frequency increments and op modes specified for NAC (C, Network Analyzer Controller) and Signal generator (S) modes.
    Enter the following on the form:

    page one:

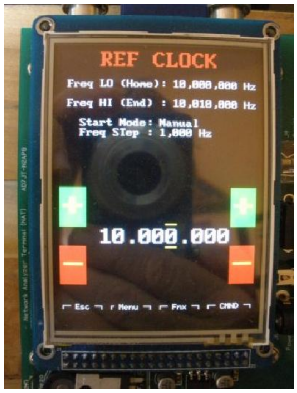
    TITLE – REF CLOCK
    FREQ LO – 10000
    FREQ HI – 10010
    FREQ ST – 1000
    leave the rest of page one blank and press Page Down to display page two

    page two:

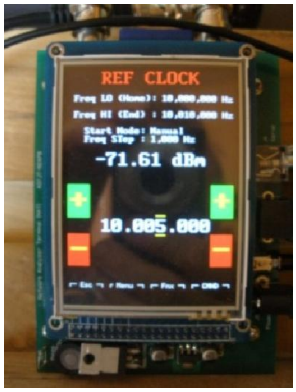
    OP MODES – CS
    leave the rest of page two blank.
3. Press Enter to save the form to EEPROM.



4. Press F1 to activate the form.
   You should now see the sig gen screen and the DDS output should be 10 MHz.



5. Press the up arrow five times to set the frequency to 10.005 MHz. For this tutorial ignore the dBm reading.



6. Tune the communications receiver to 10.005 MHz. Note, 10.005 MHz is used here to avoid QRM from WWV. If the accuracy of the communications receiver frequency dial is suspect, tune to WWV and note any frequency difference from 10.000 MHz and take the difference into account when setting the receiver frequency to 10.005 MHz.
7. Tune the receiver up and down until you hear the DDS RF output. You may need an antenna on the DDS RF output; I touch the connector with my finger and use myself for an antenna.
8. Note the actual frequency. If the frequency is less than 10.005 MHz, the reference clock frequency is set too high and must be reduced. If the frequency is greater than 10.005 MHz, the reference clock frequency is too low and must be increased.
9. Press Ctrl-T. The displayed frequency will change to the current reference clock frequency (nominally 180 MHz).

10. Use the left and right arrow keys to change the frequency step size and the up and down arrow keys to increment and decrement the reference clock frequency until it is received (zero beat) at 10.00500 MHz.

11. Press enter to save the new reference clock frequency in EEPROM.
12. Press Escape to exit Signal generator mode and end the tutorial.